data processor including:

a transformer for selectively operating on the digital signal, performing a Fast Fourier Transform, and producing frequency spectrum data from the digital signal;

a digital signal processor (DSP) connected to receive and for operating on the digital signal and independently performing Fast Fourier Transforms on the digital signal to produce a frequency spectrum; and

a central processing unit (CPU) for controlling the operation of the system including the operation of the DSP, the DSP performing the Fast Fourier Transform independently of the CPU; and

memory interfaced with the data processor for storing at least some of the digital data.

32 (new). The system of Claim 31 further comprising:

the DSP for generating a graphical representation of the frequency spectrum, and transferring the graphical representation to the memory; and

a direct memory access (DMA) for transferring data directly to the memory without interrupting the CPU, the DMA transferring data including the frequency spectrum and the graphical representation from the DSP to the memory.

33 (new). The system of Claim 31 further comprising:

the DSP for operating on and analyzing the digital signal independently of the CPU to produce an analyzed digital signal representing selected properties of the digital signal and for transmitting the analyzed digital signal to the memory independently of the CPU; and

the CPU for transmitting commands to the DSP to select the operations and analysis that is performed on the digital signal by the DSP.

34 (new). The system of Claim 33 wherein the DSP in response to commands from the CPU performs a Fast Fourier Transform independently of the CPU on the digital

signal to produce a frequency spectrum representative of the frequency content of the digital signal.

35 (new). The system of Claim 33 wherein the DSP in response to commands from the CPU performs a zoom operation independently of the CPU on the digital signal to produce a zoom digital signal representative of a selected frequency band in the digital signal.

36 (new). The system of Claim 33 wherein the DSP in response to commands from the CPU performs a low-pass filtering and decimation operation on the digital signal independently of the CPU to produce a filtered digital signal having a reduced sample rate as compared to the digital signal and being representative of a portion of the digital signal having a frequency below a selected upper frequency.

37 (new). The system of Claim 33 wherein the DSP in response to commands from the CPU performs:

a low-pass filtering and decimation operation on the digital signal independently of the CPU to produce a filtered digital signal having a reduced sample rate as compared to the digital signal and being representative of a portion of the digital signal having a frequency below a selected upper frequency;

a zoom operation independently of the CPU signal to produce a zoom digital signal representative of a selected frequency band in the digital signal; and

a Fast Fourier Transform independently of the CPU to produce a frequency spectrum representative of a frequency content of the digital signal.

38 (new). The system of Claim 31 wherein the memory further comprises:

a memory card for storing data in a card format:

a plug system for connecting and disconnecting the memory card to and from the system;

a random access memory (RAM) interfaced with the data processor for storing data; and

a RAM formatter for controlling the flow of data to and from the RAM and configuring the RAM as a pseudo-card so that the RAM in conjunction with the RAM formatter functions substantially identically as the memory card, receiving and transmitting data in card format.

39 (new). The system of Claim 31 wherein the data processor further comprises a digital filter for optionally digitally filtering the digital signal to produce a modified digital signal.

40 (new). The system of Claim 31 wherein the data processor further comprises a digital filter and decimator for optionally reducing the sample rate and frequency content of the digital signal to produce a modified digital signal.

41 (new). A data collector and analyzer system comprising:

a vibration transducer for sensing vibration and for producing an analog vibration signal corresponding to the vibration;

a conditioning circuit for receiving and conditioning the analog vibration signal from the vibration transducer to produce a conditioned analog signal, and having;

(a) a filter for producing the conditioned analog signal having a desired frequency range;

(b) an amplifier for producing the conditioned analog signal at a desired amplitude; and

(c) an analog to digital converter (ADC) for receiving and sampling the conditioned analog signal to produce a digital signal, and having:

(1) a sigma-delta modulator having a number of cascaded sigma-delta loops and having a transfer function substantially of:

$$(z) = X(z) + (1-Z^{-1})^{-n}Q^{n}(Z)$$

where Q^n is the quantization noise from the sigma-delta modulator and n is the number of cascaded sigma-delta loops,

the modulator receiving the conditioned analog signal and producing a digital modulator signal;

(2) a comb filter for digitally low-pass filtering and decimating the digital modulator signal from the modulator to produce a comb signal; and

(3) a FIR filter for digitally low-pass filtering and decimating the comb signal to produce the digital signal for the data processor;

a data processor for processing the digital signal to produce desired digital data, the data processor including:

a transformer for selectively operating on the digital signal, performing a Fast Fourier Transform, and producing frequency spectrum data from the digital signal; and

memory interfaced with the data processor for storing at least some of the digital data.

42 (new). A data collector and analyzer system comprising:

a vibration transducer for sensing vibration and for producing an analog vibration signal corresponding to the vibration;

a conditioning circuit for receiving and conditioning the analog vibration signal from the vibration transducer, and having;

a main conditioning circuit for receiving and conditioning the analog signal from the transducer to produce a conditioned main analog signal, and having;

(a) a filter having an upper cutoff frequency for producing the conditioned main analog signal having a desired frequency range;

(b) an amplifier for producing the conditioned main analog signal at a desired amplitude;

(c) a main analog to digital converter (ADC) for receiving and sampling the conditioned main analog signal to produce a

main digital signal; and

(d) a main microprocessor controller for controlling the main conditioning circuit; and

an optional conditioning circuit for receiving and conditioning the analog signal from the transducer to produce a conditioned optional analog signal, and having;

(a) a filter having an upper cutoff frequency for producing the conditioned optional analog signal having a desired frequency range;

(b) an amplifier for producing the conditioned optional analog signal at a desired amplitude; and

(c) an optional ADC for receiving and sampling the conditioned optional analog signal to produce an optional digital signal;

a data processor for processing the main and optional digital signals to produce desired digital data, the data processor including:

a transformer for selectively operating on the digital signal, performing a Fast Fourier Transform, and producing frequency spectrum data from the digital signal; and

memory interfaced with the data processor for storing at least some of the digital data.

~~43~~ (new). The system of Claim ~~42~~ wherein the main and optional conditioning circuits further comprise main and optional hardware for receiving and sampling the conditioned main analog signal and the conditioned optional analog signal, respectively, at sample frequencies that are substantially greater than maximum frequencies of interest to produce main and optional digital signals, and further for digitally low-pass filtering and digitally decimating the main and optional digital signals, respectively, to produce main and optional conditioned digital signals having reduced sample rates as compared to the main and optional digital signals, respectively, and having predetermined upper cutoff frequencies.

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44 (new). A hand held data collector and analyzer system comprising:

a main transducer for sensing analog data and for producing a main analog signal corresponding to the analog data;

an optional transducer for sensing analog data and for producing an optional analog signal corresponding to the analog data;

a main conditioning circuit for receiving and conditioning the main analog signal from the main transducer to produce a conditioned main analog signal, and having;

(a) a filter having an upper cutoff frequency for producing the conditioned main analog signal having a desired frequency range;

(b) an amplifier for producing the conditioned main analog signal at a desired amplitude;

(c) a main analog to digital converter (ADC) for receiving and sampling the conditioned main analog signal to produce a main digital signal; and

(d) a main microprocessor controller for controlling the main conditioning circuit;

an optional conditioning circuit for receiving and conditioning the optional analog signal from the optional transducer to produce a conditioned optional analog signal, and having;

(a) a filter having an upper cutoff frequency for producing the conditioned optional analog signal having a desired frequency range;

(b) an amplifier for producing the conditioned optional analog signal at a desired amplitude; and

(c) an optional ADC for receiving and sampling the conditioned optional analog signal to produce an optional digital signal;

a main digital signal processor (DSP) for receiving and selectively operating on the main digital signal, performing a Fast Fourier Transform, and producing a main frequency spectrum;

an optional DSP for receiving and selectively operating on the optional digital signal, performing a Fast Fourier Transform, and producing an optional

frequency spectrum;

a central processing unit (CPU) for controlling the operation of the system, including issuing commands to the optional DSP and the main microprocessor controller;

a main interface for connecting the CPU to the main DSP and the main microprocessor controller;

an optional interface for connecting the CPU to the optional DSP;

the main microprocessor controller for controlling the main conditioning circuit in response to commands from the CPU;

the optional DSP for controlling the optional conditioning circuit in response to commands from the CPU; and

memory interfaced with the CPU and the main and optional DSP's for storing information.

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~~45~~ (new). The system of Claim 11 ~~44~~ wherein:

the main and optional conditioning circuits further comprise main and optional hardware for receiving and sampling the conditioned main analog signal and the conditioned optional analog signal, respectively, at sample frequencies that are substantially greater than maximum frequencies of interest to produce main and optional digital signals, and further for digitally low-pass filtering and digitally decimating the main and optional digital signals, respectively, to produce main and optional conditioned digital signals having reduced sample rates as compared to the main and optional digital signals, respectively, and having predetermined upper cutoff frequencies; and

the main and optional DSP's further comprising main and optional digital low-pass filters and decimators, respectively, for optionally and selectively reducing the sample rates and frequency content of the main and optional conditioned digital signals to produce main and optional modified conditioned digital signals.

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~~46~~ (new). The system of Claim 11 ~~44~~ wherein the main DSP and the optional DSP, in

response to commands from the CPU, perform:

a low-pass filtering and decimation operation independently of the CPU to produce main and optional filtered digital signals, respectively, having reduced sample rates as compared to the main and optional digital signals, respectively, and being representative of a portion of the main and optional digital signals;

a zoom operation independently of the CPU to produce main and optional zoom digital signals, respectively, representative of selected frequency bands in the main and optional digital signals; and

a Fast Fourier Transform independently of the CPU to produce frequency spectrums representative of a frequency content of the main and optional digital signals.

14 ~~47~~ (new). The system of Claim 11 ~~44~~ wherein the optional conditioning circuit further comprises:

a separate optional circuit board; and

plug means for selectively connecting and disconnecting the optional circuit board to and from the system.

15 ~~48~~ (new). The system of Claim 11 ~~44~~ wherein:

the main and optional DSP's operate on and analyze the main and optional digital signals independently of the CPU to produce main and optional analyzed digital signals representing selected properties of the main and optional digital signals, and transmit the analyzed digital signals to the memory independently of the CPU; and

the CPU includes a direct memory access (DMA) interconnected with the main and optional DSP's and with the memory for transferring data from the main and optional DSP's to the memory without interrupting the CPU.

16 ~~49~~ (new). The system of Claim 11 ~~44~~ wherein the filter further comprises a fixed-frequency analog anti-aliasing filter.